PATENT APPLICATION
DOCKET NO. 10016350-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S): Thomas B. Pritchard **CONFIRMATION NO.:** 9419

SERIAL NO. 10/054,652 **GROUP ART UNIT:** 2622

FILED: 01/18/2002 **EXAMINER:** Milia, Mark R.

SUBJECT: SYSTEM FOR IMPROVING SPEED OF DATA PROCESSING

DECLARATION UNDER 37 C.F.R. 1.131

Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Thomas B. Pritchard state and declare that:

1. I am the inventor of currently pending claims 1 through 26 and 31 in U.S. Patent Application Serial No. 10/054,652, filed on January 18, 2002 and entitled "System for Improving Speed of Data Processing."

2. I understand that in an Office Action mailed December 29, 2005, each of currently pending claims 1-26 and 31 were rejected under 35 U.S.C. § 102(e) as being anticipated by published U.S. patent application number 2002/0122210 naming Ilbery (hereinafter referred to as Ilbery) or under 35 U.S.C. § 103(a) as obvious over Ilbery.

3. I understand, based on the information provided on the front page of Ilbery, that Ilbery was filed in the United States on December 28, 2001.

4. Prior to December 28, 2001, I conceived in the United States the invention described in currently pending claims 1-26 and 31 of the above-referenced application as evidenced by the attached Exhibit A referenced herein.

5. Exhibit A is a redacted copy of an invention disclosure having a date of submission prior to December 28, 2001, disclosing subject matter corresponding to limitations recited in currently pending claims 1-26 and 31.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: March 27, 2006 By: Thomas B. Pritchard

Exhibit A

HEWLETT PACKARD **INVENTION DISCLOSURE** PAGE ONE OF ____

PDNO 10016350 DATE RCVD [redacted] IPD ATTORNEY EAA

Instructions: The information contained in this document is COMPANY CONFIDENTIAL and may not be disclosed to others without prior authorization. Submit this disclosure to the HP Legal Department as soon as possible. No patent protection is possible until a patent application is authorized, prepared, and submitted to the Government.

Descriptive Title of Invention:

1C SCALABLE ERROR DIFFUSION

Name of Project: [redacted]

Product Name or Number: [redacted] AND [redacted] PLATFORM PRODUCTS

Was a description of the invention published, or are you planning to publish? If so, the date(s) and publication(s):

NO

Was a product including the invention announced, offered for sale, sold, or is such activity proposed? If so, the date(s) and location(s):

NO

Was the invention disclosed to anyone outside of HP, or will such disclosure occur? If so, the date(s) and name(s):

NO

If any of the above situations will occur within 3 months, call your IP attorney or the Legal Department now at 1-650-857-3061 or 408-553-3061.

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.)

JANUARY [redacted] EMAIL WITH THE SUBJECT: "RE: PWA/ASIC MEETING NOTES AND ACTION ITEMS" SENT TO ALAN LOBBAN, CORINA HALL, LUIS ABELLO, AND STEVEN MILLER.

Was the invention built or tested? If so, the date:

NO

Was this invention made under a government contract? If so, the agency and contract number:

NO

Description of Invention: *Please preserve all records of the invention and attach additional pages for the following. Each additional page should be signed and dated by the inventor(s) and witness(es).*

A. Prior solutions and their disadvantages (if available, attach copies of product literature, technical articles, patents, etc.).
B. Problems solved by the invention.
C. Advantages of the invention over what has been done before.
D. Description of the construction and operation of the invention (include appropriate schematic, block, & timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc.)

Signature of Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on this date: [[redacted]]

Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
47367	THOMAS BRENT PRITCHARD	[signature]	212-2457		IPD PLATFORM LAB

(If more than four inventors, include additional information on another copy of this form and attach to this document)

Form 3.1 IDF.PDF Rev. 11/02/98

Exhibit A

HEWLETT PACKARD **INVENTION DIS_OSURE** COMPANY CONFIDE...AL PAGE ____ OF ____

Signature of Witness(es): *(Please try to obtain the signature of the person(s) to whom invention was first disclosed.)*
The invention was first explained to, and understood by, me (us) on this date: [redacted]

Full Name	Signature	Date of Signature
Ed Tucker	Ed Tucker	[redacted]
Richard Klaus	Richard Klaus	[redacted]

Inventor & Home Address Information: *(If more than four inventors, include addl. information on a copy of this form & attach to this document)*

Inventor's Full Name

Street

City State Zip

Do you have a Residential P.O. Address? P.O. BOX City State Zip

Greeted as *(nickname, middle name, etc.)* Citizenship

Inventor's Full Name

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City State Zip

Do you have a Residential P.O. Address? P.O. BOX City State Zip

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Form 3.1 IDF.PDF Rev. 11/02/93

Exhibit A

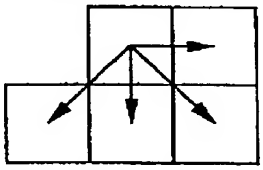
IC Scalable Error Diffusion

Summary

There is a way to make an error diffusion algorithm scalable between multiple integrated circuits, such that different ICs can be halftoning different areas of the same page simultaneously with minimal inter-IC communication overhead.

Background

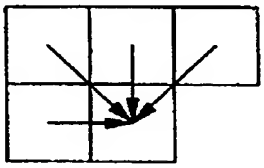
In some imaging applications, the number of bits per pixel must be reduced, but the overall intensity must be maintained. A common way of doing this is to apply an error diffusion halftoning algorithm, in which each pixel is quantized to a lower number of bits, but the error is diffused to other surrounding pixels which haven't yet been quantized. A classic example is the Floyd-Steinberg algorithm[1], published in 1976, in which the order of the processing of the pixels is in unidirectional rasters, and the error is distributed to four adjacent pixels, as follows:



This document will refer to the four diffusion directions as east, southeast, south, and southwest.

It is desirable to have a scalable solution for halftoning, such that lower performance products will cost less than higher performance products. A method of accomplishing this is to add more identical integrated circuits to perform the halftoning of multiple pixels in parallel when higher performance is required.

However, with the error diffusion algorithm as shown above, a pixel can't be calculated until all of the diffusions have been calculated from the west and three north row pixels above, as shown below:



If an attempt is made to assign different rectangular areas of the page to different ICs, and then each rectangle is processed in raster order independently, then the first northwest pixel in each rectangle can't be processed until the last southeast pixel in the rectangle to the northwest is completed, the northeast pixel in the rectangle can't be processed until the last southeast pixel is completed, etc. All of these conditions result in pixels not being able to be processed concurrently, so the goal of having a scalable solution with more ICs is not met.

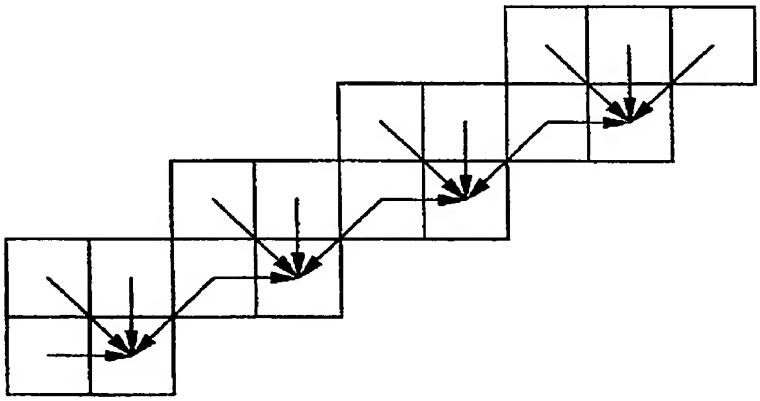
Exhibit A

Prior Solutions and their Disadvantages

One approach to solve this is to not process pixels in parallel, but instead produce new ICs which process pixels faster. If the design is an application specific integrated circuit (ASIC), then the required multiple ASIC designs take a large amount of development time and implementation cost; if the design is an off-the-shelf processor, the performance range within a processor family frequently won't be able to scale far enough, or it may be very expensive.

Another approach is to change the processing algorithm so it doesn't have the data dependencies which force the non-concurrent operation. One example of this would be to use matrix-based halftoning instead of error diffusion. Unfortunately the resulting image quality is generally not as good with these algorithms which have fewer dependencies between the pixels.

Another potential solution is to process multiple rows independently, but staggered horizontally by at least two pixels per row. An example follows with four rows processed in parallel, but this concept could be extended to any number of rows.



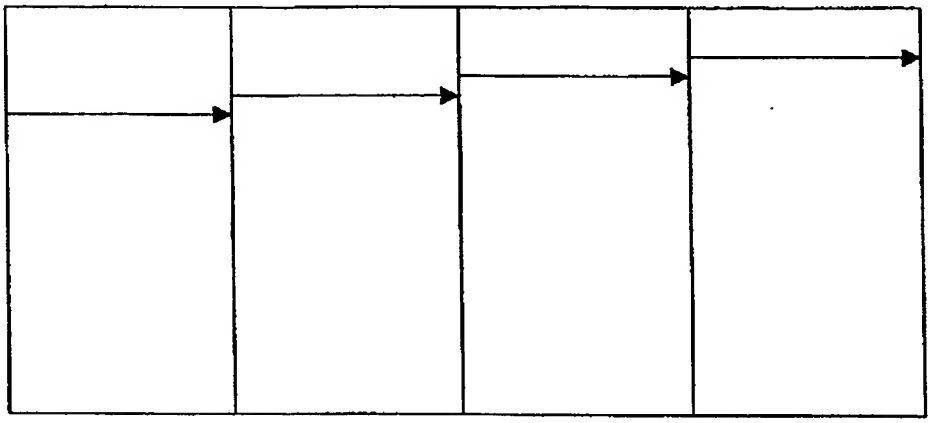
This accomplishes processing multiple pixels all in parallel, but it requires transferring between the different processing hardware the large amount of diffusion data which gets used in different rows. This may be done easily within a single processing module such as an ASIC, but a single ASIC wouldn't meet the needs of an IC scalable architecture. If multiple ICs are used, then there would have to be a high bandwidth channel between them, consuming many costly pins and generating much EMI, noise, printed circuit board space, etc.

Another approach is to have different ICs work on different pages in parallel in a multi-page document. This approach requires that full pages of data must be stored, which can be costly. Another disadvantage is that the first page won't be completed any sooner even with more added hardware.

Exhibit A

Invention

The invention involves separating the page into multiple page columns of full page height, with one IC assigned to each page column, and then processing them in staggered rows as shown (illustration shows 4 separate ICs):



When the first pixel is processed in each row for each page column, the southwest diffusion is transferred to the IC to the west (except the west-most one). And when the last pixel is processed in each row for each page column, the east and southeast diffusion values are transferred to the IC to the east (except the east-most one). Since only the pixels on the page column boundaries need to have diffusion information transferred between pixels, the amount of data is very small, so it doesn't require high bandwidth data transfers between the ICs. With the staggered rows, there can be a large latency transfer time without stalling, very close to the amount of time that it takes to process the width of a page column.

Note that this solution requires that the halftoning algorithm be unidirectional.

If there are area algorithms further down the pipeline than halftoning, then the page columns may be made to overlap, such that all of the data is available within each processing element for its output pixels.

The preferred embodiment for this invention uses the halftoning algorithm, but there are other potential uses. For example, there are certain types of infinite impulse response filter applications to which this invention may be beneficial.

[1] Described in much literature including Ulichney, R., Digital Halftoning, MIT Press, 1987, and Dougherty, Edward R., Electronic Imaging Technology, SPIE Press, 1999.